3:8 Bit CMOS Decoder Design

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Worst Case Delay: 0.523 pS
EDP: 337858 ps · pJ

I. Introduction

Decoders are devices that take binary code as inputs and use logic circuits to output a "1" at the corresponding output and "0" everywhere else. We were tasked to design a 3:8 bit decoder that minimizes the energy delay product (EDP) under the constraints of:

1. Worst case delay of 0.75ns
2. Output transition times under 300ps
3. Supply Voltage (V_{dd}) up to 1.2V
4. Complete rail-rail swing

Our design also needs to account for output load and wire capacitances as well as static CMOS inverters as input drivers.

II. Initial Estimates

We started the static CMOS design by setting the initial width and lengths of all inverters and NAND gates as 240 nm for PMOS and 120 nm for NMOS. We also set the V_{dd} =1.2 V to ensure shorter propagation delay. After a parametric sweep of the width of the PMOS and NMOS of the gates, we found the optimal widths as listed in Table 1.

Width	Inverter	NAND
PMOS	1020nm	240nm
NMOS	510nm	120nm

Table 1: Optimal Gate Sizes

We found the theoretical value of the propagation delay to be 0.405 ns and the energy dissipation to be 676.22 pJ.

$$I_D = k_n'\left(\frac{W}{L}\right)\left((V_{DD} - V_{Tn})V_{dsat} - \frac{V_{dsat}^2}{2}\right)(1 + \lambda_n V_{DD})$$

$$R_n = \frac{3}{4}\left(\frac{V_{DD}}{I_{dsatn}}\right)\left(1 - \frac{5}{6}\lambda_n V_{DD}\right)$$

$$R_p = -\frac{3}{4}\left(\frac{V_{DD}}{I_{dsat}}\right)\left(1 - \frac{5}{6}\lambda_p V_{DD}\right)$$

$$R_{eq} = R_n + R_p$$

$$t_{pLH} = 0.69\sum\left(R_{eq}C\right)$$

$$\boldsymbol{t_{pLH} = 0.405\ ns}$$

$$E = CV_{DD}^2$$

$$\boldsymbol{E = 676.22\ pJ}$$

III. Designs Tested

A. Static CMOS

We began by designing a basic decoder out of static CMOS inverters and NAND gates. The advantages of this design on energy minimization are the short propagation delay and the robustness, and the lack of leakage current. The disadvantage is the use of many transistors.

B. Pseudo-NMOS

Next we designed a decoder using Pseudo-NMOS inverters and NAND gates. The advantage of using this design is the limited number of transistors. The disadvantages, however, are the large amount of leakage current and inability to pull-down the output voltage to zero.

C. Combination

In order to reduce the number of transistors from the Static CMOS design and decrease the leakage current of the Pseudo-NMOS design we combined the two using Pseudo-NMOS NAND gates and Static CMOS inverters. Ultimately the EDP was larger than that of the Static CMOS design.

D. Other Options

We also considered using pass-transistor and dynamic logic. These however utilized a greater amount of transistors, therefore we decided they would not be better options.

IV. Static CMOS

A. Optimization

We chose to implement a Static CMOS design that consisted of inverters that are composed of two transistors and four-input NAND gates consisting of eight transistors each. This is because it allowed us to minimize energy while staying within the 300ps output transition time constraint.

In order to optimize this design we first swept the width of the inverter in a 2:1 W_p/W_n ratio. The delay was always well under 0.75ns, but to adhere to the output transition time constraint we decided to have W_p=510nm and W_n=1.02µm. These were the smallest sizes we could make the transistors and brought our worst case transition time to a 293.69ps rise time and a 233.97ps fall time.

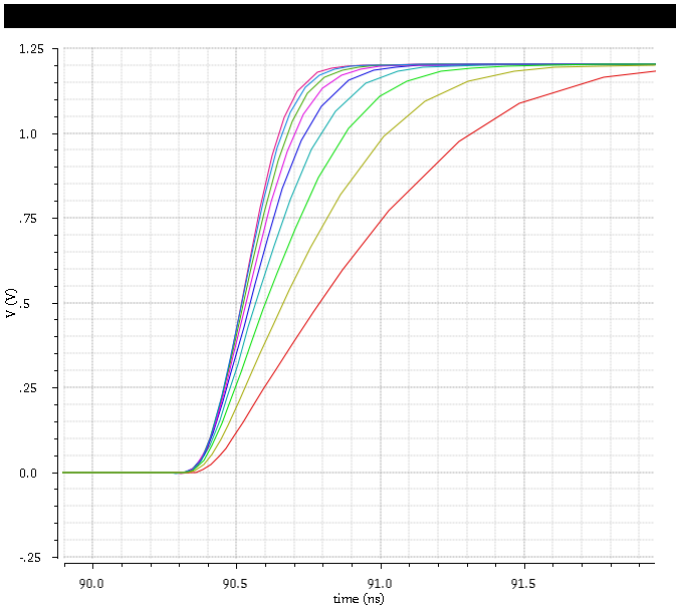


Figure 1: Sweep of Inverter Width (120nm-600nm)

We then swept the width of the NAND gate transistors in a 2:1 ratio. We found W_p=120nm and W_n=240nm to be best option, because the small sizes would keep the energy consumption lower.

Finally we swept the value of V_{dd} up to 1.2V, but we found that 1.2V was the best option because if it was any lower it would require us to increase the transistor widths to an unreasonable size.

B. Data

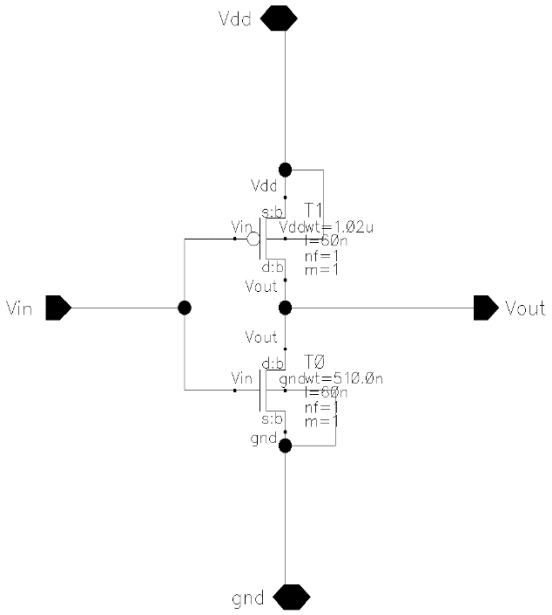
V_{dd}	1.2 V
C_{wire} (input driver)	3.9 fF
C_{wire} (inverter)	3.3 fF
C_{wire} (NAND)	1.5 fF
Worst case t_{rise} (Q_1)	293.69 ps
Worst case t_{fall} (Q_1)	233.97 ps
Energy	646 pJ
Worst case delay (Q_1)	523 ps
EDP	337858 ps · pJ

Table 2: Measured Values

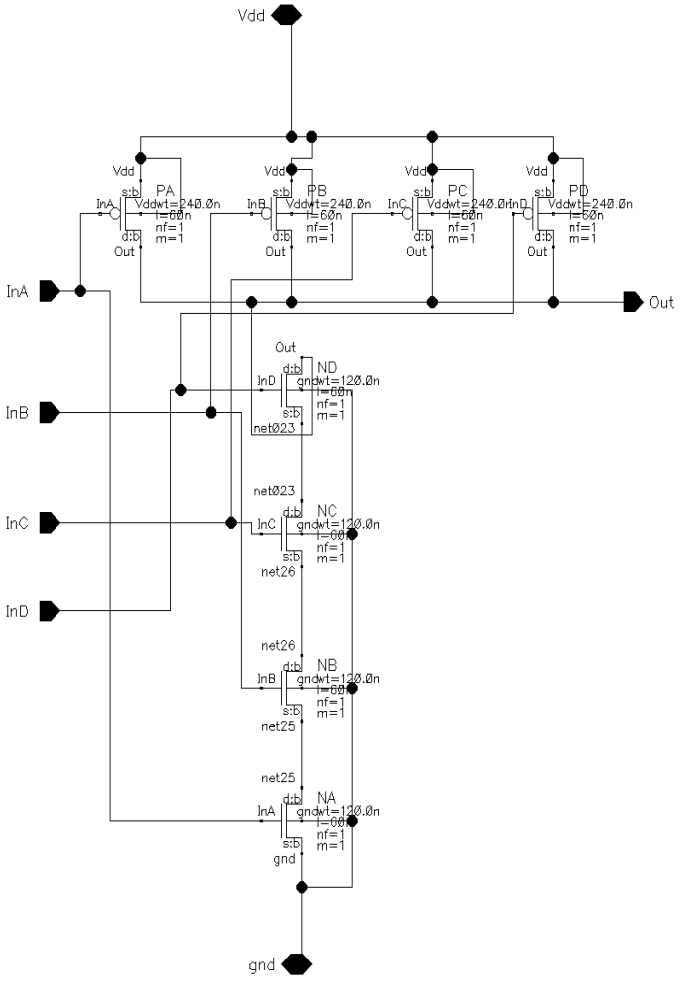
Signal	**Delay (ns)**
Q_0	0.4589
Q_1	**0.5230**
Q_2	0.4588
Q_3	0.4615
Q_4	0.4590
Q_5	0.5214
Q_6	0.4587
Q_7	0.4614

Table 3: Propagation Delays (t_{pLH})

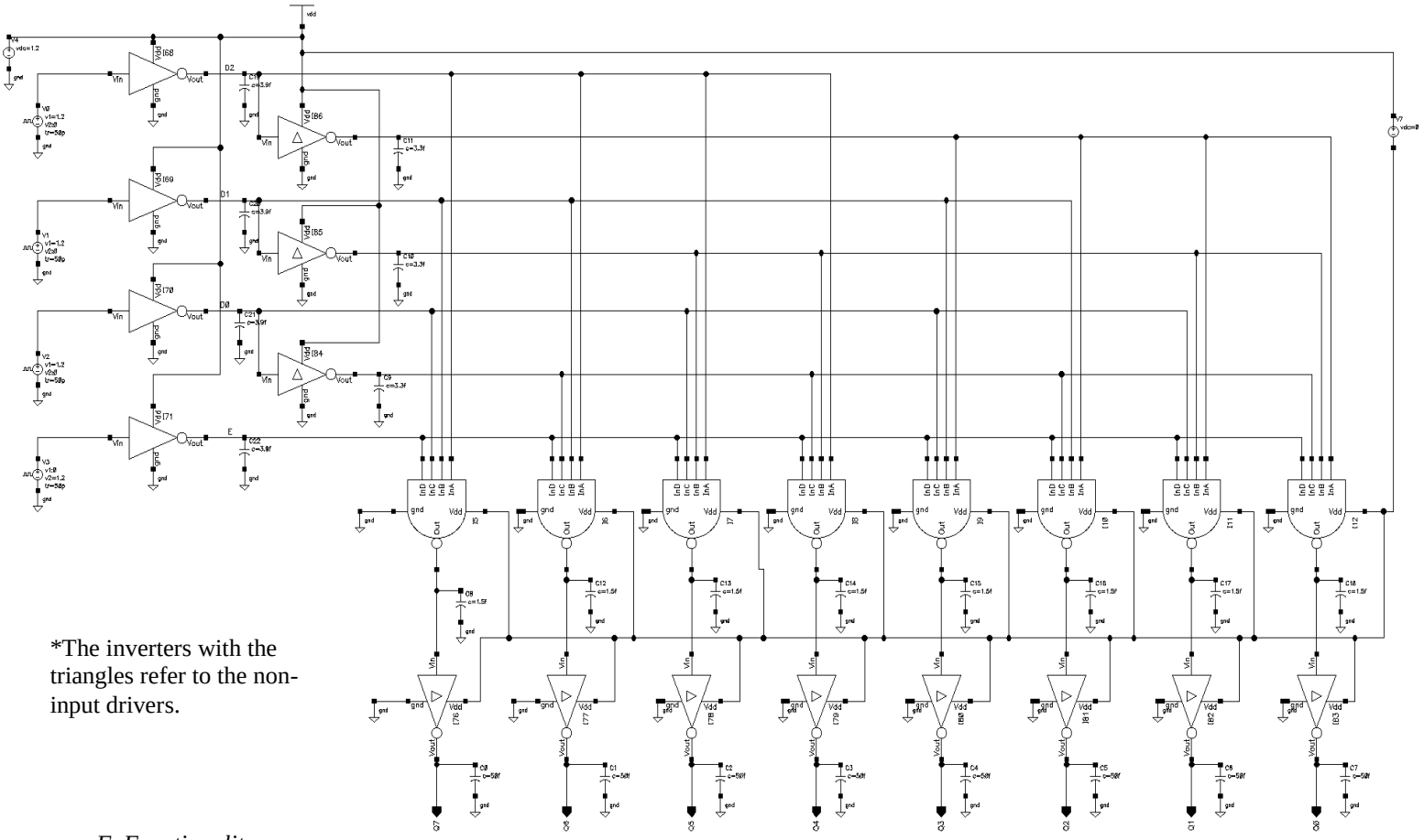
C. Inverter



D. NAND Gate

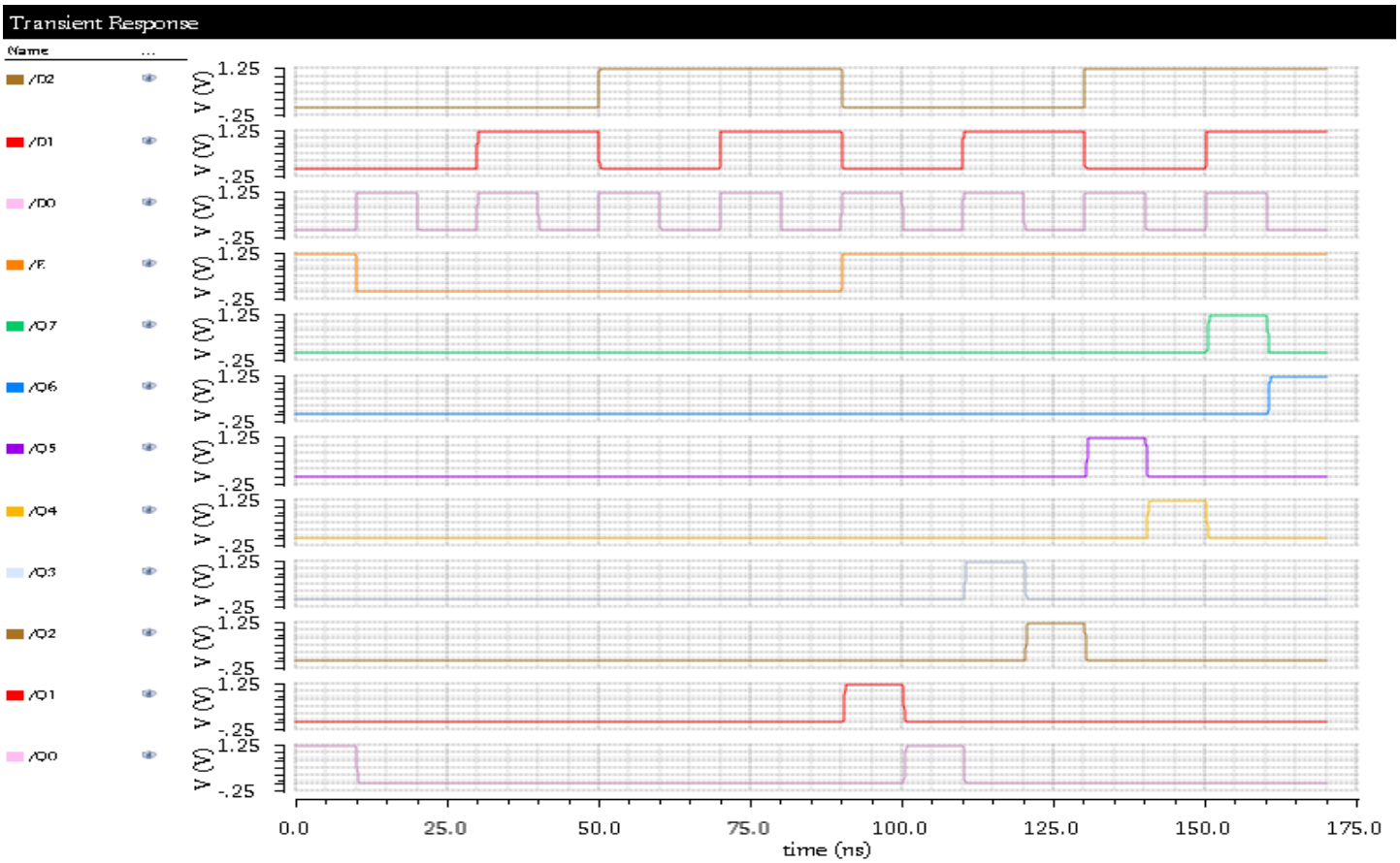


E. Decoder



*The inverters with the triangles refer to the non-input drivers.

F. Functionality



The functionality plot demonstrates the functionality of our decoder. The input patterns are based on the configurations given in the input deck.

G. Noise Margin Effectivity

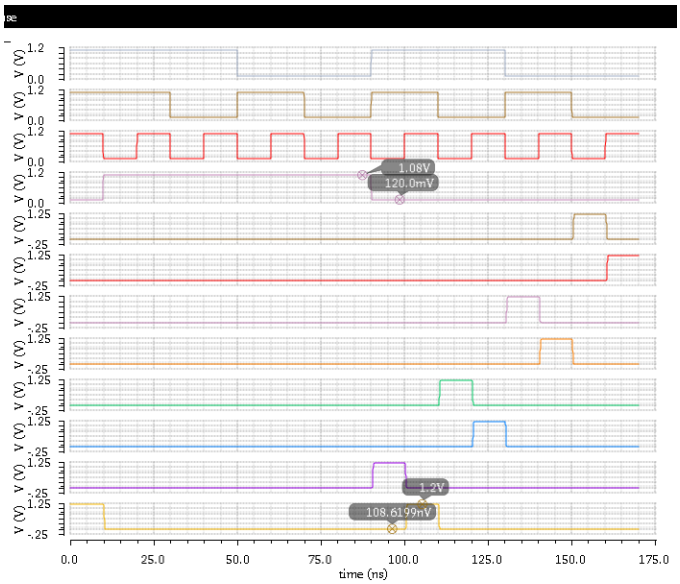


Figure 2: Robustness

Our noise margins exceed 10 percent of V_{dd}. This is evident because the output voltages still swing rail-to-rail in Figure 2, when the input pulses between $0.1V_{dd}$ and $0.9V_{dd}$.

H. Energy Dissipation

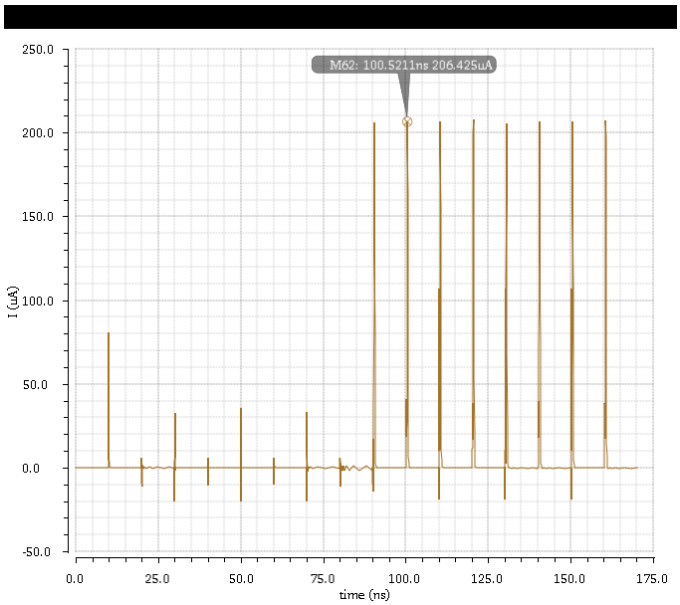


Figure 3: Current Drawn from V_{dd}

The total energy drawn from V_{dd} is 646 pJ. We found this value by first measuring the current of 0V source that we connected to the V_{dd}. Then we integrated the current over the time to find the total charge and multiplied it by V_{dd} to find the energy.

V. Conclusion

Our final 3:8 decoder design is based on the CMOS logic family. It had the smallest Energy Delay Product of 337858 ps · pJ compared to the pseudo-NMOS design and the combined design (pseudo-NMOS and CMOS). Our design is within the constraints.

The static CMOS logic family is the best choice to implement the 3:8 decoder because it is robust and it minimizes leakage current as well. Therefore, it is reliable and consumes little energy.